Priyanka Tiwari

Mailbox | Linkedin | Github

Education

Acharya Institute of Technology — Bangalore, IN
Bachelor of Engineering in Electronics and Communications Engineering — *Aug. 2023 – May 2027*

Experience

FOSSEE Summer Intern | — May 2026 – Present
IIT Bombay (FOSSEE – Free and Open Source Software for Education) — *Remote*

- Designed and implemented **ICELang**, a domain-specific language (DSL) for hardware description, enabling structured schematic definitions parsed into an abstract syntax tree (AST) with a custom lexer/parser pipeline.
- Built a **KiCad schematic export pipeline** that translates ICELang AST nodes into native KiCad `.kicad_sch` file format, automating symbol placement, wire routing, and pin mapping with ∼90% layout accuracy.
- Developed an **SVG symbol rendering engine** to visually verify schematic components pre-export, reducing debug cycle time by eliminating repeated KiCad round-trips.
- Integrated **50+ standard component symbols** (resistors, capacitors, ICs, connectors) into the ICELang symbol library, expanding DSL coverage for common circuit archetypes.
- Wrote **unit tests and integration test suites** covering lexer, parser, and exporter modules, achieving >85% code coverage and catching 12+ edge-case bugs prior to milestone submission.
- **Tech Stack:** Python, PLY (Python Lex-Yacc), KiCad Scripting API, SVG rendering, AST design patterns, Git

Projects

GXU-1: Custom GPU Co Processor | *ESP32-S3, FreeRTOS, C, React, Vite, WebSocket* | — 2026

- Architected a **custom GPU co-processor** on the ESP32-S3 featuring a handbuilt **R-2R resistor ladder DAC** for analog VGA signal output, achieving functional display output under a ***Rs.*700 BOM** .
- Designed a **custom 8-opcode binary ISA** (DRAW, FILL, CLEAR, BLIT, RECT, LINE, PIXEL, NOP) interpreted by a software rasterizer, enabling structured graphics command execution on bare metal.
- Implemented a **dual-core FreeRTOS architecture** distributing render pipeline (Core 1) and host communication (Core 0) across both ESP32-S3 cores, sustaining ∼30 FPS render throughput.
- Built a **React/Vite WebSocket dashboard** with live VRAM heatmap telemetry, opcode throughput graphs, and frame-timing visualizations for real-time GPU state introspection.
- Engineered a **browser-based software emulator** faithfully replicating the GXU-1 ISA, enabling development and testing of GPU programs without physical hardware.

Achievements

Codess Mentee — 2025
Selected for the Microsoft Codess mentorship program for women in technology

HPAIR 2026 Delegate
*Selected as a delegate for the Harvard Project for Asian and International Relations (HPAIR); placed in the **top 1%** of global app*

Technical Skills

Languages: C/C++, Python, JavaScript, TypeScript, HTML/CSS, SQL, Assembly (ESP32/Xtensa)
Embedded & Hardware: ESP32/ESP32-S3, FreeRTOS, ESP-NOW, R-2R DAC, VGA signal generation, KiCad, Ngspice, TinyML/TFLite Micro
Frameworks & Libraries: React, Vite, Next.js, Node.js, Flask, FastAPI, Supabase, pandas, NumPy, Matplotlib
AI/ML: TensorFlow Lite, on-device inference, edge AI, model quantization, split inference
Developer Tools: Git, Docker, WebSocket, VS Code, Linux, FreeRTOS, PLY (Lex-Yacc), KiCad Scripting API
Other: REST APIs, DSL design, AST construction, mesh networking, Blockchain (Hyperledger), WebGL